COMMENTS

Priority claim. The Examiner has asked that the applicant provide certified copies of Irish applications S2000/0711 and S2000/0706. The applicant never made a priority claim in this application. It is requested that the Patent Office correct its records in this regard.

Abstract. The abstract as filed did not include the title of the application. The application was filed electronically and the abstract did not include the title. If the copy of the Abstract in the Examiner's file includes the title, this is no fault of applicant and should be corrected by USPTO personnel.

Loop A and Loop B. The Examiner objects to the specification and figures because of a supposed lack of clarity as to the meaning of "Loop A" and "Loop B". In the context of FC/AL (fibre-channel arbitrated loop) disk drives, the terms "Loop A" and "Loop B" are quite well known to those skilled in the art. For example, the Examiner is respectfully referred to the co-pending related applications cited in the specification, namely the applications published as US 2002/0054477 and US 2002/0044561. (Copies of these publications are attached for the Examiner's convenient reference.)

These applications, filed by the same applicant as the present application, use like reference numerals for like components of the system. In each of these applications, see that each disk drive 80 has an "A" loop and a "B" loop. The "A" loop goes to SES_0 4 while the "B" loop goes to SES_1 4. It is thus clear that in the present application, the SES 4 of Fig. 1 receives either all of the "A" loops from the various disks 80, or it receives all of the "B" loops from the various disks 80. For one skilled in the art, then, there is no lack of clarity on this point.

This may be seen from the specification at filed paragraph 8 (published paragraph 9) where it is said that:

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> In any case, for each disk 80, each of the sending and receiving ports for loop A and loop B are brought onto a *respective* processor card 4 where they connect to a hub 6.

(emphasis added.) In other words, there is a "respective" processor card 4 for each of the loops A and B. For clarity, however, the application shows one of the loops and its respective processor card 4, while omitting the other of the loops and its respective processor card 4.

Claim 1, "first switch." The Examiner objects to claim 1 because it is supposedly unclear what is meant by "pair of switches." The Examiner asks whether the "first switch" of the claim is somehow the same as one of the two switches in the "pair of switches". The claim itself rules out any possibility that the "first switch" is somehow the same as one of the "pair of switches" because in the claim as filed, the "pair of switches" is "operatively controlled by said first switch". The specification is completely consistent on this point, stating that the "pair of switches" is the switches MUX_{S1} and MUX_{S2} (see filed paragraph 21, published paragraph 22) while the switch which controls them (the "first switch" in the claim) is switch 20 (id.).

These three distinct switches are quite clear in fig. 2.

While this appears clear to the undersigned, to remove any question for the Examiner, the claim has been amended to call these switches the "second and third" switches.

Claim 1, "said devices." To remedy the possible antecedent-basis question raised by the Examiner, two words have been added at the beginning of the claim to clarify that the loop is a "loop of devices". This provides antecedent basis for "said devices" later in the claim.

Art rejection. Claims 1-3 and 7 have been rejected as supposedly anticipated by US Pat. No. 5,991,891 to Hahn et al. ("Hahn"). As will be explained in some detail below, Hahn comes nowhere close to anticipating claim 1 and thus fails to anticipate any of the claims. Before explaining the error in the rejection, however, the undersigned will discuss the claimed invention and the disclosure of Hahn.

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The claimed invention. The claimed invention starts with a loop of devices. The loop has a particular bandwidth that is native to the particular loop technology being used.

In the claimed invention it is possible in a selective way to split the loop into two parts. After the split has occurred, some of the devices (e.g. disk drives) are in one of the two parts and the rest of the devices are in the other of the two parts. As explained in some detail in the specification, this topology change permits each loop to pass data at its full native bandwidth. The bandwidth available for getting data into and out of the system can be double the bandwidth that would be available if only a single loop were employed.

The specification compares the doubled-bandwidth performance of the split-loop system with the prior-art single-bandwidth:

> It will be seen, however, that with all devices on the same loop, the overall throughput of the host applications connected to the loop is limited to the bandwidth of the loop.

(filed paragraph 16, published paragraph 17.)

The disclosure of Hahn. Hahn is nothing more nor less than an effort to keep *all* of the devices in a loop in communication even in the event that one of the links fails. In Hahn, there is never data flowing in more than a single loop. In Hahn, a second loop is kept "idling" so that one or more of its links can, when needed, be switched into the main loop so as to preserve its status as a complete loop. This is shown for example in Hahn Fig. 3 where it is assumed that one of the links of the loop has gone bad. To overcome the problem of the failed link (shown with a large "X"), the system sacrifices the "idle" loop, appropriating two of its links to be grafted into the main loop to restore it to the state of being a complete loop. In Hahn Fig. 3 the result of this grafting of bits of the spare loop into the main loop is shown with heavy lines.

Importantly, in Hahn the bandwidth available for getting data in and out of the loop's devices is never any greater than the native bandwidth of the main loop. Nothing about Hahn ever

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rearranges loops to give rise to doubled bandwidth, a benefit of the claimed invention.

The claim language. The Examiner's attention is thus respectfully directed to that last fifty-five words of claim 1 which say:

> said second and third switches being disposed between respective port bypass circuits at which said loop is to be split so that in a first state said second and third switches *connect said devices in a single loop* and in a second state said second and third switches *divide said devices into two split loops.*

The Examiner has not quite stated what in Hahn count as the "devices" of the claim. It appears that the Examiner suggests that the "devices" are boxes 102, 104, and 106, or that the "devices" are drives 108 found within boxes 102, 104, 106. In either case, however, the Examiner has not pointed to anything in Hahn that would "divide said devices into two split loops." Indeed all of the energy and efforts of Hahn seem devoted to quite the opposite, namely a supreme effort to ensure that *all of the devices are in a single loop* no matter what catastrophe strikes the links of the loop.

It is suggested that the Examiner ought not to ignore the last fifty-five words of the claim (quoted above). Reconsideration is requested.

All the claims depending from claim 1 ought to be allowed for the same reasons. Reconsideration is requested.

Allowable subject matter. Previous claims 4-6 have been duplicated as new claims 8-10. In addition, claim 4 has been amended by adding the subject matter of claim 1. Thus it appears claims 4-6 should now be allowed.

Respectfully submitted,

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